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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/632,494	08/03/2000	Salil R. Raje	MDS-P007	1465

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EXAMINER	
LEVIN, NAUM B	
ART UNIT	PAPER NUMBER
2825	

DATE MAILED: 09/25/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/632,494	RAJE ET AL.	
	Examiner	Art Unit	
	Naum B Levin	2825	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☐ Responsive to communication(s) filed on _____ .

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *70-81,94,95 and 101-122* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *70-81,94,95 and 101-122* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *03 August 2000* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____ .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

DETAILED ACTION

1. This office action is in response to application 09/632,494 and amendment filed on 08/11/2003. Claims 70-81, 94-95 and 101-122 remain pending in the application.

2. Applicant has canceled claims 1-36, 96-100, and added new claims 101-122.

Claim Rejections - 35 USC § 102

3. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

4. Claims 70-81, 94-95 and 101-122 are rejected under 35 U.S.C. 102(e) as being anticipated by Boyle et al. (US Patent 6,557,145).

Boyle discloses method for design optimization using logical and physical information including:

(70), (76) A method for a first party to fabricate a semiconductor device, comprising: receiving a sign-off prototype, the sign-off prototype generated by (col.2, ll.15-18):

defining a physical design of a circuit while tracking an error in prediction of a timing value associated with one or more nets in the circuit (col.1, ll24-27; col.2, ll.14-21; col.3, ll.51-67; col.4, ll.1-4 and ll.54-58; col.20, ll.62-67 and col.21, ll.1-16);

determining a physical placement level of the circuit when the error in prediction of the timing value satisfies a predetermined threshold (col.4, ll.55-62 and col.6, ll.19-41); and

generating the sign-off prototype from the physical placement level of the circuit when the error in prediction of the timing value satisfies a predetermined threshold; and after receiving the sign-off prototype, the first party performing (col.2, ll.45-50 and col.5, ll.29-31):

generating a second physical design of the circuit from the sign-off prototype (col.2, ll.45-50 and col.5, ll.29-31);

generating a GDS file from the second physical design (col.2, ll.45-50 and col.5, ll.29-31);

having a mask set generated from the GDS file (col.2, ll.45-50 and col.5, ll.29-31); and

having the semiconductor device/integrated circuit fabricated using the mask set (col.2, ll.45-50 and col.5, ll.29-31);

(71), (77) The method, wherein the performing the soft placement of the design further comprises performing one or more of the following: placement of cells of the design, logic optimization of the design, routing of wires in the design, timing and clock control for the design and extraction of the design (col.1, ll.40-67; col.42 ll.1-12);

(72), (78) The method, wherein the performing the soft placement of the design further comprises simultaneously performing one or more of the following in parallel: placement

of cells of the design, logic optimization of the design, routing of wires in the design, timing and clock control for the design and extraction of the design (col.5, ll.7-31);

(73), (74), (80) The method, further comprising:

performing a second physical design of the circuit derived from the physical design of the circuit performed while tracking the error in prediction of the timing value associated with one or more nets in the circuit (col.2, ll.45-50 and col.5, ll.29-31); and

generating a GDS file from the second physical design of the circuit (col.2, ll.45-50 and col.5, ll.29-31);

(75), (79), (81) The method, wherein the determining the physical placement level of the circuit when the error in prediction of the timing value satisfies a predetermined threshold further comprises:

(a) quadrisectioning the physical design into bins/quanto-clusters (col.9, ll.40-67);

(b) localizing placement of cells and wires of the physical design into the bins (col.6, ll.50-65);

(c) creating a profile of the wire lengths in each of the bins (col.10, ll.1-6; col.11 and ll.9-40);

(d) calculating a plurality of errors in a prediction of timing values from the profile of the wire lengths for each bin respectively (col.9, ll.66-67 and col.11, ll.9-40);

(e) comparing each of the plurality of errors in the prediction of the timing values with the predetermined threshold to determine if the error satisfies the predetermined threshold; and either (col.11, ll.63-67; col.12, ll.1-5 and col.14, ll.20-38):

further quadrisectioning the physical design and repeating (b through e) (col.14, ll.39-56);

or generating an interrupt if all of the plurality of errors in the prediction of the timing values for each of the bins satisfy the predetermined threshold (col.14, ll.57-66);

(94) A semiconductor device, comprising: an integrated circuit segmented into a plurality of bins, the integrated circuit including:

a first bin having a first group of nets optimized to a first set of criteria (col.1, ll24-27; col.6, ll.50-65; col.9, ll.40-67 and ll.66-67; col.10, ll.1-6; col.11, ll.9-40 and ll.63-67; col.12, ll.1-5 and col.14, ll.20-38); and

a second bin having a second group of nets optimized to a second set of criteria, wherein the first criteria and the second criteria are substantially different (col.14, ll.39-56);

(95) The semiconductor device of claim 94, wherein the first bin is designed to a first GDS level and the second bin is designed to a second GDS level (col.1, ll24-27; col.6, ll.50-65; col.9, ll.40-67 and ll.66-67; col.10, ll.1-6; col.11, ll.9-40 and ll.63-67; col.12, ll.1-5 and col.14, ll.20-38 and ll.39-56);

(101) A method of performing a design of a circuit, comprising:

accessing a gate level design for said circuit (col.1, ll.63-67);

creating a physical prototype from said gate level design, said creating of a physical prototype/pre-layout includes predicting of timing for said circuit and tracking an error (timing hot spots/slacks) in said predicting of timing (col.2, ll.1-4; col.2, ll.13-20; col.3, ll.51-67; col.4, ll.1-4 and ll.54-58; col.5, ll.7-17; col.20, ll.62-67 and col.21, ll.1-16); and

creating a physical design for said circuit, said creating of said physical design includes placing and routing elements of said circuit, said creating of a physical prototype is performed prior to said creating of said physical design (col.2, ll. 16-34 and ll.45-50 and col.5, ll.21-23 and ll.29-31);

(102) A method according to claim 101, wherein:

said step of creating a physical design is performed using a physical design tool (col.7, ll.35-59); and

said step of creating a physical prototype is performed without using said physical design tool (col.2, ll.13-15; col.5, ll.7-17);

(103) A method according to claim 101, wherein said creating of said physical prototype comprises:

localizing placement of cells and wires (col.6, ll.50-65);

creating a profile of wire lengths (col.10, ll.1-6; col.11 and ll.9-40);

calculating an error in a prediction of a timing value from said profile of said wire lengths (col.9, ll.66-67 and col.11, ll.9-40);

comparing said error in said prediction with a predetermined threshold (col.11, ll.63-67; col.12, ll.1-5 and col.14, ll.20-38); and

performing further placement if said error does not satisfy said predetermined threshold (col.2, ll.44-46);

(104) A method according to claim 101, wherein said creating of said physical prototype comprises:

defining a representation of said circuit based on said gate level design (col.1, ll.63-67);

quadrisectioning said representation into bins (col.9, ll.40-67);

localizing placement of cells and wires of said representation into said bins (col.6, ll.50-65);

creating a profile of wire lengths in each of said bins (col.10, ll.1-6; col.11 and ll.9-40);

calculating a plurality of errors in a prediction of timing values from said profile of said wire lengths for each bin respectively (col.9, ll.66-67 and col.11, ll.9-40);

comparing each of said plurality of errors in said prediction of said timing values with a predetermined threshold (col.11, ll.63-67; col.12, ll.1-5 and col.14, ll.20-38); and

if said error does not satisfy said predetermined threshold, further quadrisectioning said representation and repeating said steps of localizing, creating, calculating and comparing (col.2, ll.44-46; col.14, ll.39-56);

(105) A method according to claim 101, wherein said creating of said physical prototype further comprises analyzing congestion and power for said physical prototype (col.1, ll.24-27; col.6, ll.46-48; col.15, ll.66-67 and col.16, ll.1-9);

(106) A method according to claim 101, further comprising: generating a GDS file from said physical design (col.2, ll.45-50 and col.5, ll.29-31);

(107) A method according to claim 101, further comprising (col.2, ll.45-50 and col.5, ll.29-31): generating a GDS rule from said physical design; having a mask set generated from the GDS file; and having the semiconductor device fabricated using the mask set.

(108), (113), (118) A method, computer readable medium with code and computer system for performing a design of a circuit, comprising (col.8, ll.10-35; col.20, ll.62-67 and col.21, ll.1-10):

accessing a gate level design for said circuit (col.1, ll.63-67);

creating a physical prototype from said gate level design, said creating of a physical prototype includes predicting of timing for said circuit (col.2, ll.1-4; col.2, ll.13-20; col.3, ll.51-67; col.4, ll.1-4 and ll.54-58; col.5, ll.7-17; col.20, ll.62-67 and col.21, ll.1-16); and

providing said physical prototype for a physical design process so that a physical design can be created for said circuit including placing and routing elements of said circuit, said creating of a physical prototype is performed prior to said step of providing (col.2, ll. 16-34 and ll.45-50 and col.5, ll.21-23 and ll.29-31);

(109), (114), (119) A method, computer readable medium with code and computer system, wherein:

said step of providing includes providing said physical prototype to a physical design tool (col.7, ll.35-59); and

said step of creating a physical prototype is performed without using said physical design tool (col.2, ll.13-15; col.5, ll.7-17);

(110), (115), (120) A method, computer readable medium with code and computer system, wherein said creating of said physical prototype comprises:

localizing placement of cells and wires (col.6, ll.50-65);

creating a profile of wire lengths (col.10, ll.1-6; col.11 and ll.9-40);

calculating an error in a prediction of a timing value from said profile of said wire lengths (col.9, ll.66-67 and col.11, ll.9-40);

comparing said error in said prediction with a predetermined threshold (col.11, ll.63-67; col.12, ll.1-5 and col.14, ll.20-38); and

performing further placement if said error does not satisfy said predetermined threshold (col.2, ll.44-46);

(111), (116), (121) A method, computer readable medium with code and computer system, wherein said creating of said physical prototype comprises:

defining a representation of said circuit based on said gate level design (col.1, ll.63-67);

quadrisectioning said representation into bins (col.9, ll.40-67);

localizing placement of cells and wires of said representation into said bins (col.6, ll.50-65);

creating a profile of wire lengths in each of said bins (col.10, ll.1-6; col.11 and ll.9-40);

calculating a plurality of errors in a prediction of timing values from said profile of said wire lengths for each bin respectively (col.9, ll.66-67 and col.11, ll.9-40);

comparing each of said plurality of errors in said prediction of said timing values with a predetermined threshold (col.11, ll.63-67; col.12, ll.1-5 and col.14, ll.20-38); and

if said error does not satisfy said predetermined threshold, further quadrisectioning said representation and repeating said steps of localizing, creating, calculating and comparing (col.2, ll.44-46; col.14, ll.39-56);

(112), (117), (122) A method, computer readable medium with code and computer system, wherein said creating of said physical prototype further comprises analyzing

congestion and power for said physical prototype (col.1, ll.24-27; col.6, ll.46-48; col.15, ll.66-67 and col.16, ll.1-9).

REMARKS

5. Examiner appreciates the detailed remarks offered by Applicant. However claims do not recite these specific particular limitations.

6. Mostly, the Applicant argues "The cited prior art ... and ...There is no disclosure in Boyle et al. of creating a physical prototype prior to creating the physical design, as recited above in claim 101".

Boyle, for example teaches prior art (Fig.1): "... Based on this initial partition, the circuit partitioning step in layout step 112 further refines circuit partitions down to the l level of individual "cells" (e.g., logic gates or macro cells). ...The cells so placed are then routed to provide the necessary interconnect. ... This optimization cycle is repeated until all timing problems are resolved, represented by the post-layout sign-off step 114.Test patterns can then be generated in an automatic test pattern generation (ATPG) step 116, and the final layout design can then be manufactured." (Col.2, ll.21-50).

So prior art already discloses creating post-layout or "physical prototype" in terms of Application, and final layout or "physical design" as described in Application. Post-layout/"physical prototype" is created prior final layout/"physical design" as claimed in Application.

Additionally Boyle teaches: "One embodiment of the present invention is a design method 200 illustrated in FIG. 2. ... Method 200, however, synthesizes layout using a

novel concurrent design optimization step 209, which performs in parallel placement, logic optimization and routing functions driven by concurrent timing and power analyses. ... post-layout sign-off step 114 and ATPG step 116 can be performed in the conventional manner." (col.5, ll.7-31).

So Boyle's invention also teaches creating post-layout or "physical prototype" in terms of Application, and final layout or "physical design" as described in Application. Post-layout/"physical prototype" is created prior final layout/"physical design" as claimed in Application.

7. With respect to claims 94-95 the Applicant argues that Boyle does not discloses following limitations of above claims: "a first group of nets optimized to a first set of criteria... a second bin [has] a second group of nets optimized to a second set of criteria, wherein the first criteria and the second criteria are substantially different."

Boyle recites: "Typically, layout design tasks include, generally, the steps of circuit partitioning, placement and routing. As mentioned above, an initial circuit partition based on the gate-level design is already provided at floor-planning step 103. Based on this initial partition, the circuit partitioning step in layout step 112 further refines circuit partitions down to the level of individual "cells" (e.g., logic gates or macro cells). These cells are then placed according to some **constraints, which are typically expressed by a cost function. Typical constraints relate to area, power and local timing. The cells so placed are then routed to provide the necessary interconnect. The routing is also typically performed according to certain constraints, such as local timing and power constraints**." (col.2, ll.21-33).

So Boyle's invention also teaches partitioning/"segmented" integrated circuit in individual cells/"bins", and optimization of routing using different constraints/cost functions/"criteria", as claimed in Application.

8. Accordingly, **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Conclusion

9. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Naum B Levin whose telephone number is 703-305-0144. The examiner can normally be reached on M-F (8:00-4:30).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Matthew S Smith can be reached on 703-308-1323. The fax phone number for the organization where this application or proceeding is assigned is (703) 872-9306.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is 703-308-0956.

N L

LEIGH M. GARBOWSKI
PRIMARY EXAMINER